Track Reconstruction with Deep Learning at the CERN CMS Experiment

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Connecting the Dots

/ the CERN openlab summer school I am participating in the Intel Modern Code Developer Challenge. The scope of this challenge is to write a couple of technical posts about our projects at CERN to share part of our work with the Intel developer community.

In the following weeks I will describe in detail the results of my project, including

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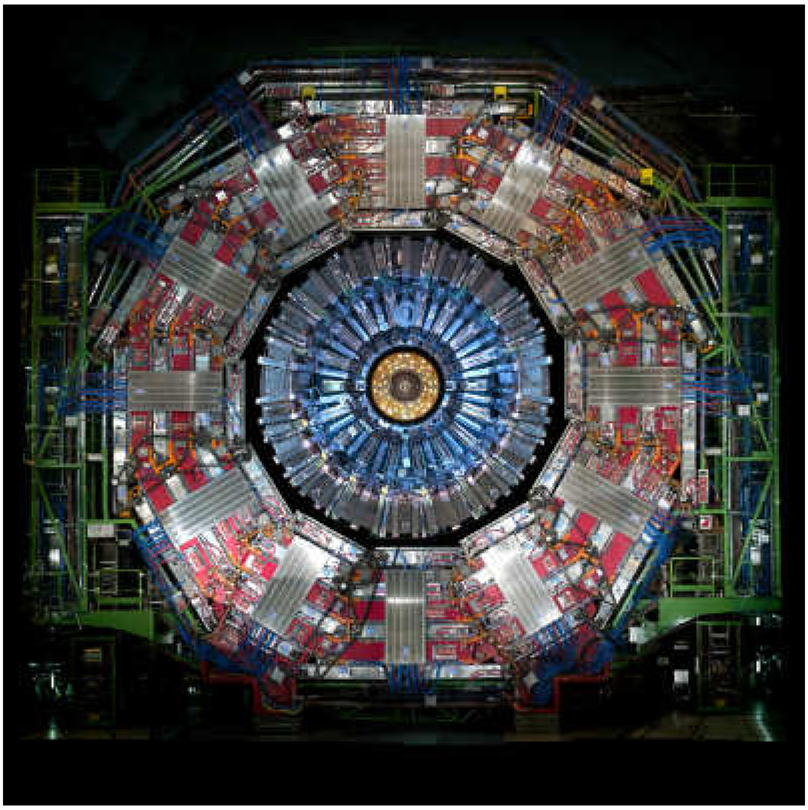
CERN

The european center for nuclear research (CERN) is located in Geneva, Switzerland, where the LHC(Large Hadron Collider), the biggest particle accelerator in the world, is built in a 27 km tunnel built 100 m underground . Inside the accelerator two proton beams are accelerated through various stages in opposite direction until they reach a velocity close to the speed of light and they collide with a center of mass energy of 13 TeV. From these collisions new particles are generated that are recorded with particle detctors and their properties are studied by the phisicists to unveil new particles or better understand their properties. There are four main experiments at the LHC but I will talk only about CMS, which is the one where I am working on.

CMS

The Compact Muon Solenoid (CMS) is a general purpose detector used to detect particles generated by proton-proton collisions. It is composed of many cilindrical layers. The innermost part is the silicon tracker, divided in two subdetectors, the pixel tracker and the strip tracker. It is designed to identify the particle's trajectories with high precision and it is made entirely of silicon to endure the high level of radiation inside the detector. The internal subdetector, the pixel tracker, is made of small square sensors while the external subdetector, the strip tracker, is made of rectangular strips. Both sensors are capable to detect charged particle. After that we have the calorimeter, used to detect the particle's energy. The next layer is the superconducting solenoid, which generates a 4T magnetic field. The magnetic field is used to bend the they are used to recognize muons.



Each detector generates a huge amount of data. A new collision happen every 25 ns and the detector record about 1 PB/s of data from the collisions. This data are filtered because they cannot be entirely stored in persistent memory. Fortunately only a small fraction of the events are interesting for analysis. A first filter, called the L1 trigger, select events based on simple signatures, for example the presence of high-energy particles. This first coarse filter reduces the rate of events to 1 MHz. The next step is the HLT (High Level Trigger) that performs more

To select the interesting events in the HLT it is necessary to reconstruct the trajectory of each particle and in order to do that the raw data from the silicon tracker is processed to recover the trajectories.

The silicon tracker is made of several cilindrical layers centered around the interaction region. The first four layers of the tracker are part of the pixel tracker and are made of milions of pixel channels that emit electrons when a charged particle traverse them. This electrons are read with fast electronics in the detector and sent to the L1 trigger.

In the HLT raw data from the detector is processed to obtain hit clusters, which are formed by nearby pixels which have an ADC value greater than zero. The cluster shape depends both on the particle, on its trajectory and on the module that has been hit.

Track reconstruction by its nature is a combinatorial problem because given a partial track formed by hits found in the internal layers there could be multiple hits compatible with the current track estimation and they must be checked because we don't want to lose any track

It is implemented as an iterative algorithm where each iteration apply the following steps:

- seed generation
- track finding
- track fitting
- track selection

In the seed generation track seed are created from hits found in the internal layers of the detector. A set of parameters determines the compatible hits that can form a track, like the set of compatible layers or the window in each layer to use to find the hits. The seeds found in the first step are used for the track finding, which looks for other hits in the outer layers. After all the hits have been associated to the track the track fitting determines the parameters of the trajectory. The last step of the iteration is track selection, which is necessary because the previous steps could generate fake tracks. This steps looks for signals that denotes fake particles, like a large number of missing hits. Note that missing hits could be caused by different reason, like broken pixels or a region not covered by sensors (e.g. the region between two different modules).

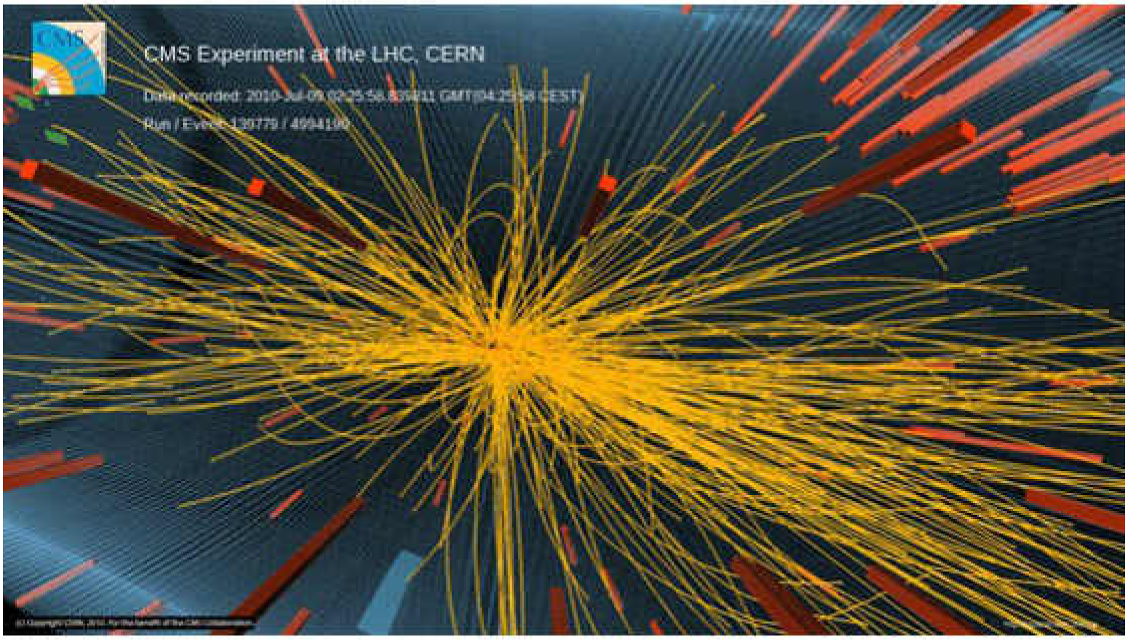
easy tracks first, eliminate from the successive searches the hits associated with the found tracks, and look for the more difficult tracks in the successive steps with a less dense environment.

Pileup

The main problem of this approach is the huge number of fake track generated during the seed generation and track finding. This is worsened by the fact that multiple collisions happens at each bunch crossing, a phenomenon called pileup (PU). Today about 25 collisions happen at each bunch crossing. In 2025 the HL-LHC (High Luminosity LHC) will become active and it will produce 10 times more data, with a pileup of 250. This means that the number of hits will increase accordingly and the number of fake tracks will exponentially explode.

The current algorithms and hardware are not capable of handling that amount of data and must be improved to overcome this upcoming challenge.

One of the most promising solution is the parallelization of the algorithms. This approach requires a complete redesign of the algorithms, which must be adapted to support vectorization or execution on



Doublet filtering

The objective of my project is to reduce the number of fake tracks as soon as possible to avoid to perform useless computation afterwards. To achieve this goal we are trying to filter out the bad track seeds, those which are not part of a real track. In particular we are developing a machine learning model based on convolutional neural networks which will take as input two hit clusters as well as some additional information about them like their global coordinates and some ID to identify the exact module inside the detector where the hit resides and outputs the probability that the two hits correspond to a real track. This model can

A good model will need to satisfy these two requirements:

- It should be precise. In practice we want to keep at least 99% of the true tracks
- It should be fast. The model must be capable to filter the doublets in real time

Both requirements are hard constraints that cannot be reduced. If we lose too many seeds we reduce the quality of the data, undermining all the subsequent analysis that will be performed offline with the stored data.

On the other side, if the inference is too slow the model cannot be used during the data collection and it is useless.

To tackle this problem we are looking at different solutions, both on the software side and on the hardware side.

On the software side, we are trying different frameworks, like Caffe*, TensorFlow* and neon™.

There are also specific network, like binarized neural network, which are designed to be much faster than standard neural network but require specialized different hardware solutions, like manycore, GPUs and FPGAs. In particular we plan to do extensive benchmarking with the Intel® Xeon Phi™ processor and Intel's new FPGA architecture specialized for machine learning inference.

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Source:https://software.intel.com/en-us/blogs/2017/08/17/track-reconstruction-with-deep-learning-at-the-cern-cms-experiment

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By Promotion Published Date 24 - Aug - 2017 | Last Updated 24 - Aug - 2017

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we've been busy planning meet ups and dev labs for the remainder of the year. If you missed out on what we and our developers have been doing, here is a rundown of all the happenings.

OpenStack* Seventh Birthday Celebration

On July 27, Intel hosted the OpenStack* seventh birthday party. The meetup was held in the auditorium of the Intel Altera campus.

Presenters from the Linux Foundation* and Intel were featured, and speakers and attendees had the opportunity to attend

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(Intel partners). The closing session of the day was the keynote given by Uri Elzur, CTO, Intel. Uri talked about the "Meaningful and Necessary Operation on behalf of NFV and MANO". The evening birthday celebration kicked off with lightning talks from the sponsors of the day: Intel, Kumulus Technologies*, Cisco DevNet*, Datera*, Mirantis*, Rackspace*, Trilio*, VMware* and the OpenStack Meet-up* groups from the San

Francisco Bay Area and San Diego. Sujata Tibrewala used the lightning

talk to discuss platform optimizations for Intel® Xeon® processor with vector event can be found on the SF Bay Area OpenStack User Group YouTube Channel.

Welcome New Intel® Software Innovators

Three new Intel® Software Innovators on-boarded from attendees of Fast Packet Processing in VNF Using DPDK and fd.io Tutorial at IEEE SDN Net soft (July, Italy)

Shohreh Ahvar, PhD student, Institut Mines Telecom, Telecom SudParis in co-accreditation with the Pierre and Marie Curie University (Paris 6) on the topic of cloud-based content delivery networks working on Ericson-funded projects. Her research interests are network function virtualization, content delivery networks, cloud computing and wireless sensor networks.

Mohammad Shojafar, Senior researcher at the University of Rome Tor Vergata to work on the 5G Superfluidity project (Consorzio Nazionale Interuniversitario per le Telecomunicazioni), Rome, Italy.

Marco Spaziani Brunella, Research associate for CNIT/University of Rome Tor Vergata. Background in RTL system design and is currently focused on CPU architectures for network packet/flow processing.

Platform Transformation for NFV and SDN

Come learn about some of the technologies that are instrumental in the platform transformation for NFV and SDN.

28 August 2017 – Portland, OR

Reality of SDN, OpenStack EPA and Containers

Stephen Hemminger, principal software engineer at Microsoft and a Linux* developer is the featured speaker at the next Portland meet up.

As maintainer of the Linux bridging and the iproute2* utilities, Stephen contributes regularly to the Linux kernel and DPDK projects.

7 September 2017 – Portland, OR

Intel® Builders Developer Summit

Please join us for the Intel Builders Developer Summit, where you'll hear directly from Intel architects and engineers on topics spanning the data center, from cloud and fabric, to network and storage. The summit's full-day technology from the sessions.

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19-20 September 2017 – San Jose, CA

Intel® Developer Zone SDN/NFV Network Developer Lab

Call for demos and talks is open. Email your proposal before September 1, 2017.

Hands-on Labs planned

OpenStack EPA (Enhanced Platform Awareness with Network Services Benchmark example VNFs)
OpenStack OpenDaylight*
New model for cloud network function development: YANFF (yet another network function framework)
Demo: Kuryr + OpenDaylight that provides the ability to deliver networking for virtual machines (VM) and containers that enable microservices
The lab is free to attend but you must apply for consideration.

6-8 November 2017 – Berlin, Germany

Manohar Castilino, Eric Ernst (both from Intel) and Shohreh Ahvar, Intel Innovator).

6-8 November 2017 – Berlin, Germany IEEE Conference on Network Function Virtualization and Software Defined Networks

Tutorial: Fast Packet Processing Towards Scalable and Agile VNFs. Speakers: Sujata Tibrewala, Muthurajan Jayakumar, Manohar Castelino , and Sundar Vedantham.

This tutorial is part of Berlin 5G week

At our meet ups, you will interact with and learn from experts at the forefront of the SDN and NFV revolution. Register for our hands-on labs and tech talks, and participate in our on-site network developer challenges for cool prizes. For more information, go to Out of the Box Network Developers.

New on Intel® Developer Zone (Intel® DZ)

Check out the following new content and more at the Intel Developer Zone Networking site.

videos:

Intel Clear Containers Overview, featuring Amy Leeland
Intel Clear Containers: How We Made Them Smaller and Faster Part 1, featuring Manohar Castelino
Intel Clear Containers: How We Made Them Smaller and Faster Part 2, featuring Manohar Castelino
The Open vSwitch* Exact-Match Cache

The Exact-Match Cache is the first and fastest mechanism used by Open vSwitch* (OVS) to determine what to do with an incoming packet. See its role in the OVS workflow and learn about its key features.

Get Started with IPsec* Acceleration in the FD.io VPP Project.

Learn how FD.io, VPP, and the DPDK Cryptodev library work together to provide enhanced IPsec* performance and functionality. Configuration instructions are included.

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